REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendment and the following remarks.

By the foregoing amendment, claims 1, 6 and 7 have been amended. Claims 11-29 have been withdrawn from consideration. Thus, claims 1-10 are currently pending in the application and subject to examination.

In the Office Action mailed February 21, 2007, claims 1-10 were rejected under 35 U.S.C. § 102(e) as being anticipated by Preiss et al., U.S. Patent No. 6,757,763 (hereinafter, "Preiss"). It is noted that claims 1, 6 and 7 have been amended. To the extent that the rejection remains applicable to the claims currently pending, the Applicant hereby traverses the rejection, as follows.

The communication control information of Preiss, that is txfifo_do and txfifo_empty are sent by not a sending side device but TXFIFO (FIG.4). TXFIFO detects the internal states in terms of hardware and sends txfifo_do and txfifo_empty to make a notice of the detected internal states.

Independent claims 1 and 6 are directed to an inter-bus communication interface device for controlling data communication between a first bus and a second bus. Independent claim 7 is directed to an information processing unit for carrying out information processing in cooperation with an external host apparatus connected thereto via an external connection bus.

Independent claim 1 as amended, recites, among other features, a buffer for storing only communication data sent from a first device connected to the first bus and a register for storing only communication control information concerning the

communication data sent from the first device for handling the communication data. A control circuit passes the communication data stored in the buffer to a second device connected to the second bus, and passing the communication control information stored in the register to the second device, and the second device performs an appropriate receive process according to the control information.

Independent claim 6 as amended, recites, among other features, a first buffer for storing only first communication data sent from a first device connected to the first bus; a first register for storing only first communication control information concerning the first communication data sent from the first device for handling the communication data; a second buffer for storing only second communication data sent from a second device connected to the second bus; a second register for storing only second communication control information concerning the second communication data sent from the second device for handling the communication data; and a control circuit for passing the first communication data stored in the first buffer to the second device, and the first communication control information stored in the first register to the second device, and further passing the second communication data stored in the second buffer to the first device, and the second communication control information stored in the second register to the first device; wherein the first device and the second device perform an appropriate receive process according to the control information.

Independent claim 7 as amended, recites, among other features, an internal CPU; a receive buffer for storing only receive data received from the external host apparatus; a receive register for storing only receive communication control information concerning the receive data from the external host apparatus for handling the receive

data; a transmit buffer for storing only transmit data transmitted from the internal CPU via an internal bus; a transmit register for storing only transmit communication control information concerning the transmit data from the internal CPU for handling the transmit data; and a control circuit for passing the receive data stored in the receive register to the internal CPU and passing the receive communication control information stored in the receive register to the internal CPU, and further passing the transmit data stored in the transmit buffer to the external host apparatus and passing the transmit communication control information stored in the transmit register to the external host apparatus; wherein the internal CPU and the external host apparatus perform an appropriate process according to the control information.

In each of claims 1, 6 and 7, as amended, the communication control information is information that the first device of the sending side sets according to the communication states for the communication control that is performed by the receiving side device. The sending side device (e.g., the CPU performing communication control) directly sends the communication control information to the receiving side device via the register according to the communication states, thereby directing the communication control processing. This eliminates the need for the receiving side device to analyze the contents of data to extract communication control information. As a result, data reception can be efficiently performed.

In Preiss, the communication control information txfifo_do and txfifo_empty are sent by TXFIFO (see Fig. 4) and not by a sending side device. TXFIFO detects the internal states in terms of hardware and sends txfifo_do and txfifo_empty to make a notice of the detected internal states. In Preiss, communication control information is

not generated unless the memory region of the FIFO becomes a prescribed hardware state, for example, full or empty. Therefore, to perform the communication control by using such communication control information, hardware conditions for generating a control signal should be satisfied by performing a prescribed process such as by making the FIFO full of dummy data. Further, it is difficult to direct communication control by using the generated signal only, and therefore instructions have to be separately embedded in data to be transferred via a buffer.

Preiss does not disclose or suggest at least the combination of a register for storing only communication control information concerning the communication data sent from the first device for handling the communication data; and a control circuit for passing the communication data stored in said buffer to a second device connected to the second bus, and passing the communication control information stored in said register to the second device; wherein the second device performs an appropriate receive process according to the control information, as recited in claim 1, as amended.

For at least this reason, the Applicant submits that claim 1, as amended, is allowable over the applied art of record. As claim 1 is allowable, the Applicant submits that claims 2-5, which depend from allowable claim 1, are likewise allowable for at least the reasons set forth above with respect to claim 1.

The Applicant further submits that independent claims 6 and 7 are allowable for reasons similar to claim 1. As claim 7 is allowable, the Applicant submits that claims 8-10, which depend from allowable claim 7, are likewise allowable for at least the reasons set forth above with respect to claim 7.

Conclusion

For all of the above reasons, it is respectfully submitted that claims 1-10 are in condition for allowance and a Notice of Allowability is earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is invited to contact the undersigned representative at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300 referencing client matter number 107337-00106.

Respectfully submitted,

Arent Fox LLP
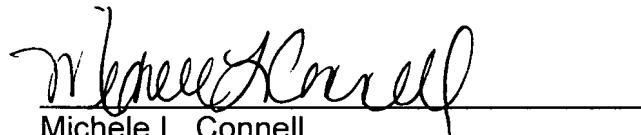
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Enclosures: Petition for Extension of Time (two months)